# Analysis and Design of On-sensor ECG Processors for Realtime Detection of VF, VT, and PVC

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***Abstract*—Cardiovascular disease remains the main cause of death, and great efforts are spent on the design of ECG body sensors these years. Essential components such as analog frontend and wireless transceivers have been integrated on a compact IC with micro-Watt power consumption. To provide timely warning against the fatal vascular signs, based on the Chaotic Phase Space Differential (CPSD) algorithm, on-sensor processors are implemented to detect the abnormal ECG for VF, VT and PVC. The on-sensor processing reduces 98.0% power of wireless data transmission for raw ECG signals. The application specific processor is designed to accelerate CPSD algorithm with 1.7$\mu$W power while the OpenRISC is integrated to provide the system flexibility. The architecture is realized on the FPGA platform to physically demonstrate the detection of the abnormal ECG signals in a real time.**

## I. Introduction

The world population is aging rapidly. It is crucial to provide adequate health care for the elders. Heart disease is one of the most prevailing and dangerous diseases among others of longevity, and remains by far the main cause of death. More than 5,000 people, for instance, experience sudden cardiac arrest (SCA) every week in the US. The chance for survival drops 10 percent per minute without defibrillation, and more than 95 percent of SCA victim die [1]. Thus it is of great interest to provide timely warning against fatal vascular signs.

Efforts are spent on body sensors these years to support the need in the healthcare applications [2]. To build a practical realtime heart status monitoring and analyzing system, several design requirements should be considered. Compact form factor and low power consumption are two primary issues for the mobile or wearable devices. In addition, to provide timely warning against the SCA, the system demands essential computation capability to perform signal processing algorithms in a real time. Flexibility should also be provided to adjust the algorithm parameters for different individuals and circumstances, which may easily disrupt the system robustness otherwise.

Most commercial ECG holters utilize off-the-shelf components and have the lifetime less than 12 hours. Due to the advance in silicon technology, the components are being integrated on chip to reduce the form factor and power consumption. The analog frontend modules including the amplifier, filter, and ADC were first implemented on a single IC and consume micro-Watt power [3]. A wireless transceiver and programmable digital controllers were further integrated as a system on chip (SoC) for the complete sensor node [4]. Such encapsulated sensor node could be realized in the form of a thin and flexible patch, and is capable of transmitting ECG signals wirelessly for days. Afterwards, more digital features were explored on chip for more functionalities. To provide point-of-care capability, a sub-threshold general purpose processor (GPP) was embedded on the sensor node, and the heart rate calculation was demonstrated with 2.6 $\mu$W power [5]. Transmitting the raw data wirelessly dominates the power consumption on sensor node. Application specific processor (ASP) was thus implemented to compress and encrypt the ECG raw signals [6] in order to further save the power.

In this paper, on-chip digital system is implemented to distinguish the normal ECG rhythm from the Ventricular Fibrillation (VF) as well as the Premature Ventricular Contraction(PVC) in a real time. Patients with PVC are at higher risk for future heart attacks as well as other cardiovascular diseases. VF may cause sudden cardiac death. The proposed system can not only record a cardiac healthy reference but also make an alarm during the SCA. The remainder of this paper is organized as follows. Section II briefly reviews our algorithm that previously developed and tested with human ECG data in [7]. In Section III, the architecture utilizing HW/SW co-working with both GPP and ASP is designed to achieve the optimized performance in terms of power efficiency and flexibility. The implementation results as well as the FPGA demonstration are shown in Section IV, and Section V concludes this work.

## II. Algorithm

In most cases, the mechanism of SCA onset is a Ventricular Tachycardia(VT) that rapidly progresses to Ventricular Fibrillation(VF) [8]. The Chaotic Phase Space Differential (CPSD) algorithm [7] has been developed to continuously detect critical cardiac conditions (i.e., VF,VT) based on the time-delayed phase space reconstruction method. Further, the CPSD algorithm can also distinguish other abnormal cardiovascular sign such as Premature Ventricular Contraction(PVC) according to the extracted feature from the ECG signal.

Figure 1(a)–(g) shows the illustration of CPSD algorithm. In training mode, the algorithm finds an steady ECG window of length $W$ seconds as the reference. And in testing mode, it compares the current signal with the reference to obtain the index of variation. The signal $s(t)$ in the window

$$W(t_{current}) = \{t_i \mid t \in [t_{current} - W + d, t_{current}]\} \quad (1)$$

is plotted in a diagram in the following steps.

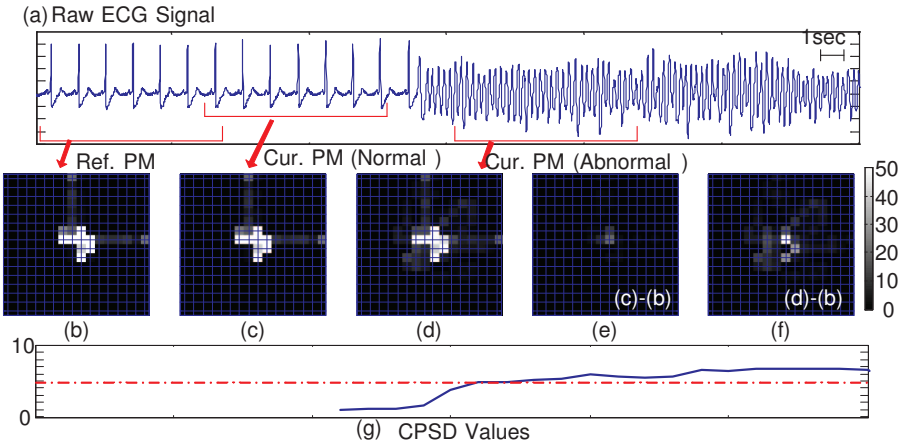


Fig. 1. The illustration of CPSD algorithm. (a) is the ECG signal derived from normal into VF. (b) is the phase space matrix constructed from normal ECG signal in the training state and served as a reference in the testing stage. (c) is the phase space matrix constructed from normal ECG signal in testing, while (d) is the phase space matrix constructed from VF ECG signal in testing.(e) and (f) shows the difference phase space matrix of (b)-(c) and (d)-(c), respectively. An typical VF ECG signal spreads out on the phase space while normal ECG signal does not. (g) shows the corresponding CPSD value and threshold for VF.

*1) Construct the phase vectors:* The phase space vector $\vec{v}$ is obtained by the delayed signal pairs.

$$\vec{v}(t_i) = \langle s(t_i - d), s(t_i) \rangle, t_i \in W(t_{current}) \tag{2}$$

*2) Quantize the phase vector:* Quantize each dimension of the vector into $N$ levels based on $M$ to get $v^*(t_i)$.

$$\begin{aligned} &v^*(t_i) = \langle \lfloor \tfrac{(s(t_i-d)+M)N+M}{2M} \rfloor, \lfloor \tfrac{(s(t_i)+M)N+M}{2M} \rfloor \rangle, \\ &t_i \in W(t_{current}) \end{aligned} \tag{3}$$

where $M = max(s(t_i)), t_i \in W(t_{reference})$ is the maximum absolute value in the reference window. Note that signal in current window is saturated into $[-M, M]$ after a valid reference has been found.

*3) Construct the phase space matrix:* The phase space matrix $PM$ is built based on the histogram of these quantized vectors.

$$\begin{aligned} &PM_{t_{current}}(j,k) = \|\{i \mid v^*(t_i) = \langle j,k \rangle, \\ &t_i \in W(t_{current}), j,k \in \{0,1,2,...,N-1\}\}\| \end{aligned} \tag{4}$$

*4) Compute the difference phase space matrix:* The number of difference between two matrix can serve as an index of variation of the signal.

$$\begin{aligned} &Diff(PM_{t_{current}}, PM_{t_{reference}}) = \|\{(j,k) \mid \\ &|PM_{t_{current}}(j,k) - PM_{t_{reference}}(j,k)| > h, j,k \in \{0,1,2,...,N-1\}\}\|, \end{aligned} \tag{5}$$

where $h$ is the threshold of difference.

*5) Compute the CPSD value:* The final CPSD index is calculated by

$$CPSD = \frac{Diff(PM_{t_{current}}, PM_{t_{reference}})}{Diff(PM_{reference+1}, PM_{reference})}, \tag{6}$$

In the above steps, the algorithm requires a reference phase space matrix that is suitable for each individual. The algorithm adaptively generates a reference phase space matrix during each trial instead of deriving it from databases. In the training stage, a candidate phase space matrix corresponding to signal in $W(t_{candidate})$ is constructed, and is then compared to a checking phase space matrix corresponding to signal in $W(t_{candidate+1})$. If the difference satisfies

$$Diff(PM_{candidate+1}, PM_{candidate}) < Threshold_{valid}, \tag{7}$$

the candidate phase space matrix becomes a valid reference phase matrix, and remains its value throughout testing stage. If the candidate fails the test, the signal in the next window would serve as the candidate. The reference is updated in a period of 30 seconds to track the variation of the reference signal. Generally, the training stage takes 8-9 seconds upon started, and takes 1-2 seconds in retraining. The reference signal collected and validated in real-time makes the algorithm adapted to each individual during each trial.

Figure 1(a),(g) shows an typical VF signal and the corresponding CPSD value. To distinguish different cardiovascular diseases from the CPSD value, a set of thresholds along with other parameters were optimized and described in [7]. According to [7], the statistical results of PVC, VF/VT from MIT arrhythmia databases [9] showed that the CPSD algorithm successfully identified PVC, VF/VT with sensitivity and specificity greater than 95%. Besides detecting fatal signs, the CPSD value can also serves as an index of interest in the further processing of ECG signal such as compression, storage, transmission, and other detailed analysis. Hence, it is an algorithm suitable for heart status monitoring system.

There are several parameters in the CPSD algorithm, such as window length $W$, matrix size $N$, constant time delay $d$ between two dimensions in the phase vectors etc. In practice, it is of great merit to retain flexibility in the system. For example, the threshold of difference $h$ between reference matrix and current matrix should be larger in the presence of large background noise.

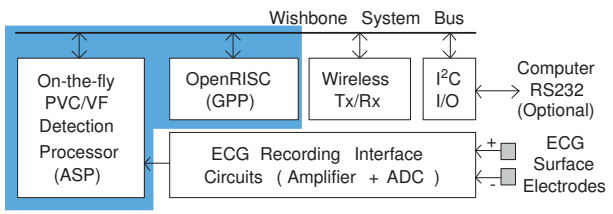


Fig. 2. The architecture of the proposed system with the on-chip ASP and GPP.

## III. Architecture

### A. System Architecture with On-chip ASP and GPP

Figure 2 shows the architecture of the proposed system. The ECG signals are amplified and digitized by the analog recording interface circuit, and then input to the digital section sample by sample. The digital section has two processors. The CPSD processor is an application specific processor (ASP) extracting the CPSD values on-line from the raw ECG samples. Afterwards, the OpenRISC, a 32-bit general purpose processor (GPP), is used to decide if there is a fatal sign or not based on the extracted CPSD values. User interfaces such as the wireless transceiver and an $I^2C$ port are connected via the wishbone system bus and are controlled by the GPP.

Two levels of power reduction are achieved with this system hierarchy. First, in the traditional design, the sensor node transmits the raw ECG signals to the base node where the processing is generally performed. However, transmitting the raw ECG signals wirelessly consumes a significant power in this case. We move the computing load from the base node to the sensor, and trade the transmission power with the computation power through the on-chip signal processing. After the signal processing, the raw data could be sent only if a fatal ECG sign is detected. The transmitter can stay asleep or send only the extracted features in the normal situation.

The second level of power reduction focuses on the on-chip signal processing. The processing on raw ECG signals such as filtering, vector extraction, and matrix operation has great requirement on data accessing. Utilizing the GPP for these operations requires continuous data fetching and storing between SRAMs and registers, and is less efficient in power consumption. We utilize both the ASP and GPP in our system to reflect the need of the application. To improve the power efficiency, the ASP is designed to accelerate the CPSD algorithm with the customized memory hierarchy and parallel processing units. The GPP can thus be operated with a much lower operation frequency and provide the flexibility for the system. Except the final decision of the CPSD algorithm, the GPP can also be programmed to decide the response after the detection of the fatal ECG sign. In addition, the algorithm and hardware parameters such as the threshold value and the gain of the amplifier can also be adjusted by GPP if required.

### B. Module Architecture of CPSD ASP

Figure 3 shows the architecture of CPSD ASP. The inputs are the 10-bit bit-parallel sample-serial ECG samples from the ADC. The outputs are the CPSD values. The CPSD is generated once per second and can be retrieved by GPP through the

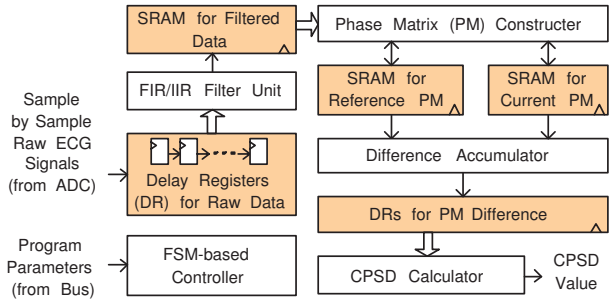


Fig. 3. The block diagram of the integrated ASP for CPSD acceleration.

TABLE I
Implementation Results of Digital Section in 90 nm CMOS Process

| Process | 90 nm 1P9M Low Leakage CMOS | |
|---|---|---|
| Supply Voltage | 1.0 Volt | |
| | CPSD ASP | OpenRISC GPP |
| Gate Count | 18050 | 32214 |
| Operation Frequency | 100 KHz | 4KHz |
| Power Consumption | 1.704$\mu$W | 3.823$\mu$W |

interrupt interaction. The ASP has four processing pipelines, and the ECG samples keep streaming through the pipeline buffers for CPSD operations. This customized structure avoids the redundant data fetching and results in the low power consumption.

A filter unit is placed in the first pipeline to remove the low-frequency drifting voltage and the 60Hz power line noise. The filter is designed with cascaded multiply-accumulate (MAC) units, and the filter coefficients are able to be programmed through the system bus. An SRAM is used to store an 8-sec window of the filtered ECG samples after the filtering. In the second pipeline, the Phase Matrix Constructer scans through the SRAM of the filtered data, extracts the phase vectors, and then constructs the corresponding phase matrix (PM) in the PM SRAMs. The third pipeline compares two PM in the PM SRAMs and accumulates the differences. The last pipeline calculates the CPSD value with the two latest PM differences according to eq. 6.

The ASP has two operation phases—the training phase and on-line processing phase. After the system reset, the training phase finds the reference PM according to eq. 7 as the normal ECG pattern specific for each user. After the training, the ASP enters the online processing phase and keeps comparing the current PM with the reference one. Note that the retraining can be activated to adapt the change of the environment by the GPP if required.

## IV. Implementation and Comparison

### A. Implementation Results and FPGA Demonstration

The proposed digital system is implemented with verilog language and synthesized in 90nm low-leakage CMOS process. Table I summarizes the implementation results.

We physically demonstrate the system with FPGA platform (Xilinx xc5vlx110X) as shown in Fig. 4. The ECG signals are first amplified and filtered by the in-house instrument

TABLE II
POWER ANALYSIS OF DIFFERENT ARCHITECTURES

(Unit:$\mu W$)

| | No Processing | GPP Only | ASP Only | Proposed | Proposed ASP + sub-Vt GPP |
|---|---|---|---|---|---|
| Amplifier | 1.55 | 1.55 | 1.55 | 1.55 | 1.55 |
| ADC | 0.41 | 0.41 | 0.41 | 0.41 | 0.41 |
| GPP | / | 423.11 | / | 3.82 | 0.0015 |
| ASP | / | / | 1.70 | 1.70 | 1.70 |
| Wireless Tx | 107.11 | 0.67 | 0.67 | 0.67 | 0.67 |
| Total | 109.07 | 425.74 | 4.33 | 8.16 | 4.34 |

amplifier IC. Then the A/D converter on FPGA board converts the analog ECG into digital samples at 256 samples per second (sps). Afterwards, the digital samples are input to the proposed digital system with ASP and GPP for the CPSD calculation. The filter coefficients programmed in ASP are designed to support an 1–100 Hz band pass filter and two notch filters around 60 Hz and 120 Hz. The programming is done through the $I^2C$ port in this demonstration. The CPSD value is computed by the ASP while thresholding of the CPSD value is performed by the GPP. The FPGA is connected to a laptop with RS-232, and the filtered raw data as well as the CPSD index are fetched and displayed with GUI on the screen.

### B. Comparison

The power consumption between different systems of the sensor node is compared in Table II. The power of amplifier and ADC is referred to [5] while the power of wireless transmission unit is referred to [4]. The power is scaled to fit the scenario of sampling resolution at 10 bit and 256 sps. Since the transmitter can be turned off dynamically by the GPP, we assume the wireless Tx power is in proportional to the transmission data rate. According to the GNU GCC compiler of the OpenRISC, 4 MIPS computation complexity is required if the whole CPSD algorithm is performed by the GPP in a real time. 0.423 mW power consumption is thus required according to the synthesized results.

In the case of no processing on chip, the sensor node continuously sends the raw ECG samples to the base node, and the processing is done on the base node. In this case, 98% of power consumption is consumed by the wireless Tx unit on the sensor node. The power consumption of wireless transmission can be reduced using on-chip processing. However, if only the GPP is integrated, because of its poor power efficiency for the data stream processing, a larger power of 425.7$\mu$W is required, which conflicts the main purpose of the design. If the algorithm is implemented with an ASP. The power consumption is significantly reduced by 98.9% as shown in the third column. However, this architecture lacks the flexibility and may violate the application requirements. In the proposed architecture with both ASP and GPP, because the main routine is performed by the ASP, the GPP can work with a lower operation frequency, and provide the essential flexibility with only 3.82$\mu$W power. There exists another dimension of optimization. In [5], Jocke et.al. implemented a sub-threshold digital microcontroller with the power efficiency of 1.51pJ per instruction. If this sub-threshold digital microcontroller is utilized in the proposed system, the power consumption can be reduced to 4.34 $\mu$W.

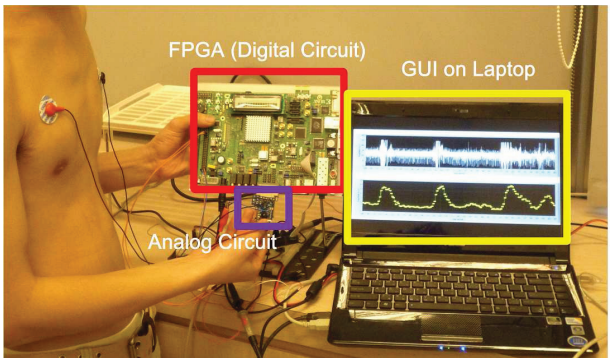


Fig. 4. The ECG signals are amplified and filtered by the in-house instrument amplifier IC. Then the A/D converter on FPGA board converts the analog ECG into digital samples at 256 samples per second (sps). Afterwards, the proposed digital system with ASP and GPP performs the CPSD calculation. The FPGA is connected to a laptop with RS-232, and the filtered raw data as well as the CPSD index are fetched and displayed with GUI on the screen.

## V. CONCLUSION

In this paper, on-sensor ECG processors are designed for the realtime heart monitoring and analysis SoC to give a timely warning against the fatal vascular signs. The system consists of an ASP to accelerate the CPSD algorithm as well as a GPP to control the system and provide the flexibility. Different architectures are discussed and compared, which leads to the conclusion that processing on the sensor node can reduce 98% power of wireless transmission for the raw ECG signals. Also the ASP can be used to incorporate with GPP and reduce the power consumption of the GPP by 99%. Such HW/SW coworking is a trade-off between processing efficiency and flexibility, and the proposed system achieves an optimized balance through the careful analysis.

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